AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows.

Please change the title of the specification as follows:

-- SEMICONDUCTOR DEVICE HAVING AN ELEMENT ISOLATING INSULATION FILM --

On page 3 of the specification please amend the paragraph beginning at line 11 as follows:

Accordingly, the polycrystalline silicon film must be doped with impurities of a predetermined conductivity type before formation of the source/drain diffusion layer. That is, ~~separates~~separate ion implantation steps are required to form the source/drain diffusion layer and to dope the polycrystalline silicon film with impurities of a predetermined conductivity type, thereby increasing the number of required steps.

On page 23 of the specification please amend the paragraph beginning at line 11 as follows:

Next, as shown in FIG. 1E, the surface of the epitaxial layer 3 remaining in the element forming regions is etched about 10 to 50 nm to remove a crystal damaged layer formed on the surface of the epitaxial layer 3 in the step of FIG. 1D. As [[s]]a result, the surface of the epitaxial layer 3 is below a surface of the thermal oxide film 2.

On page 25 of the specification please amend the paragraph beginning at line 9 as follows:

When MOS transistors were measured for threshold voltage with respect to gate processing size (gate length), the threshold voltage was found to ~~decreases~~decrease significantly in a short channel region.

Page 31 of the specification, please amend the paragraph bridging pages 31 and 32 as follows:

FIGS. 4A to 4K are process sectional views showing a method for manufacturing a MOS transistor according to a fourth embodiment of the present invention. First, as shown in FIG. 4A, a thermal oxide film 22 of thickness between about 200 and 300 nm is formed on a monocrystalline silicon substrate 41 by means of thermal oxidation. After the thermal oxidation, NO, N_2O, NH_3, or nitrogen radicals may be used to replace a SiN film for a region of the thermal oxide film 22 at least about 10 to 20 nm deep from its surface.

On page 32 of the specification, please amend the paragraph beginning at line 8 as follows:

Next, as shown in FIG. [[6A]]4A, photolithography and anisotropic etching are used to selectively remove those portions of the thermal oxide film 22 that correspond to element forming regions, and an epitaxial layer 23 is then grown so as to be thicker than the thermal oxide film 22 and to extend upward above the film 22. Next, as in the second embodiment, a silicon film 24 is formed all over the epitaxial layer 23 to eliminate the pattern dependency of the thickness of the epitaxial layer 23.

On page 36 of the specification, please amend the paragraph beginning at line 19 as follows:

The thermal treatment for activation of the impurities is desirably started by producing a vacuum in a thermal treatment room or allowing a sufficient amount of inert gas such as N or Ar to flow through the thermal treatment room so that an oxidizing agent such as oxygen, water vapor, or carbon dioxide will not enter the room. FIG. 4I shows a sectional view after the thermal treatment.

On page 43 of the specification please amend the paragraph beginning at line 18 as follows:

First, as shown in FIG. 6A, thermal oxidation is used to form an oxide film 42 of thickness about 200 nm on a surface of a ~~monocrytal~~monocrystal silicon substrate 41, and the CVD process is used to form a silicon nitride film 43 of thickness about 50 nm on the oxide film 42. The silicon substrate 41 has a p conductivity type and a face orientation (100).

On page 56 of the specification, please amend theparagraph beginning at line 25 as follows:

With a structure of step amount $\delta \leqq 0$, the step amount $\delta \leqq 10$ nm is preferred, as described below.

Page 61 of the specification, please amend the paragraph beginning at line 22 as follows:

Fig. 19A is a top view of a MIS type semiconductor element and its peripheral planar configuration. FIG. 19B is a sectional view taken along a line 19B-19B[[']] in FIG. 19A. FIG. 19C is a sectional view taken along a line [[19]]C—[[19]]C[[']] in FIG. 19[[B]]A.

Page 61 of the specification, please amend the paragraph bridging pages 61 and 62 to read as follows:

In these figures, reference numeral 71 denotes a semiconductor substrate (a silicon substrate or the like), reference numeral 72 denotes an element isolating insulating film of the STI structure, reference numeral 73 denotes a gate insulating film, reference numeral 74 denotes a gate electrode, reference numerals [[75a and 76a]] 15a and 15b denote source and drain regions (extension regions) containing impurities of a relatively low concentration, reference numerals 75b and 76b denote source and drain regions containing impurities of a relatively high concentration, and reference numeral 77 denotes a side wall insulating film formed on side walls of the gate electrode 74. The gate electrode 74 is, for example, a metal gate electrode, a polysilicon gate electrode, a polymetal gate electrode, or a polycide gate electrode.

Page 66 of the specification, the paragraph beginning at line 25, please amend as follows:

Although in the example shown in FIGS. 19A to 19C, the projections [[20]] are separated by the isolating insulating film [[12]], the adjacent projections may be connected together at one or more points. That is, the channel regions each formed in a corresponding one of the adjacent projections have only to be separated by the isolating insulating film formed in the corresponding recess, and the projections 20 are not necessarily be completely separated mutually. By connecting the adjacent projections together in an appropriate region other than the

corresponding adjacent channel regions, the source regions mutually separated in the example in FIGS. 19A to 19C can be formed into a common source region, while the drain regions mutually separated in the same example can be formed into a common drain region. By providing a common source region and a common drain region, electrodes can be led from these regions easily.